Cipher-201
Hardware Reference Manual

V1.1

September 1, 1999

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2. Preface

This manual provides in-depth hardware informations of the Cipher-201 programmable terminal and serves as a reference for hardware and maintenance engineers. Assumption has been made that readers of this manual have basic knowledge of electric and/or electronic theory.

Numberings of all components, including connectors, passive and active components conforms to the PCB V3.01. However, Syntech does not guarantee this conformity. The numberings and locations of components might be re-arranged. For confirmation, please refer to the PCB and its schematics. After all, this manual intends to describe the operation theory of the circuitry utilized.

3. General Features

The Cipher-201 is equipped with the follows,

- TLCS-900 16 bit CPU running at 9.8304 MHz
- Program : 128 KB flash memory
- Data memory : 32 or 128 KB SRAM
- Optional Fine-tunable calendar chip
- Memory & calendar chip backup 3.6V NiCd battery
- 2 reader ports for barcode Wand, Laser-emulation scanners or up to dual-track magnetic card reader.
- optional 2 X 20 characters dot-matrix LCD display with adjustable back-light and viewing angle
- optional 4 X 4 membrane keypad
- 2 digital input ports
- 2 digital output ports
- external keyboard port (AT keyboard) or keyboard emulation
- 3 serial communication ports, depending on ports, can be configured as RS232, CMOS RS232 or RS485

4. Characteristics

Basic characteristics of the Cipher-201 are listed below,

4.1. Electrical

- Main Power Supply Voltage :
  - 8 to 20 V DC from DC-jack
  - +5V from C1 or C2
- Power consumption : 0.5W maximum without LCD nor external devices attached

4.2. Environmental

- Humidity (operating) : non-condensed 20% to 90%
- Humidity (storage) : non-condensed 10% to 95%
- Temperature (operating) : 0 to 50
- Temperature (storage) : -20 to 70
- EMC regulation : FCC class A and CE approved

4.3. Physical

- Dimensions : 179 * 116 * 32 mm (without LCD)
- Weight : 300 gram maximum (without LCD)
- Material : ABS
- Color : Gray

5. Nomenclature

The overall out-looking and connector locations are depicted below,

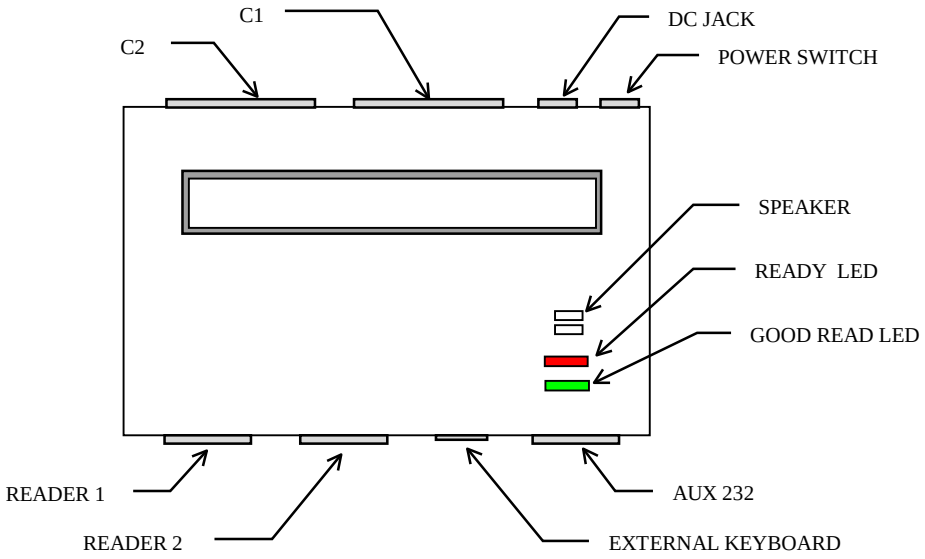


Figure 1. Nomenclature

6. PCB

The PCB and locations of major components are shown below,

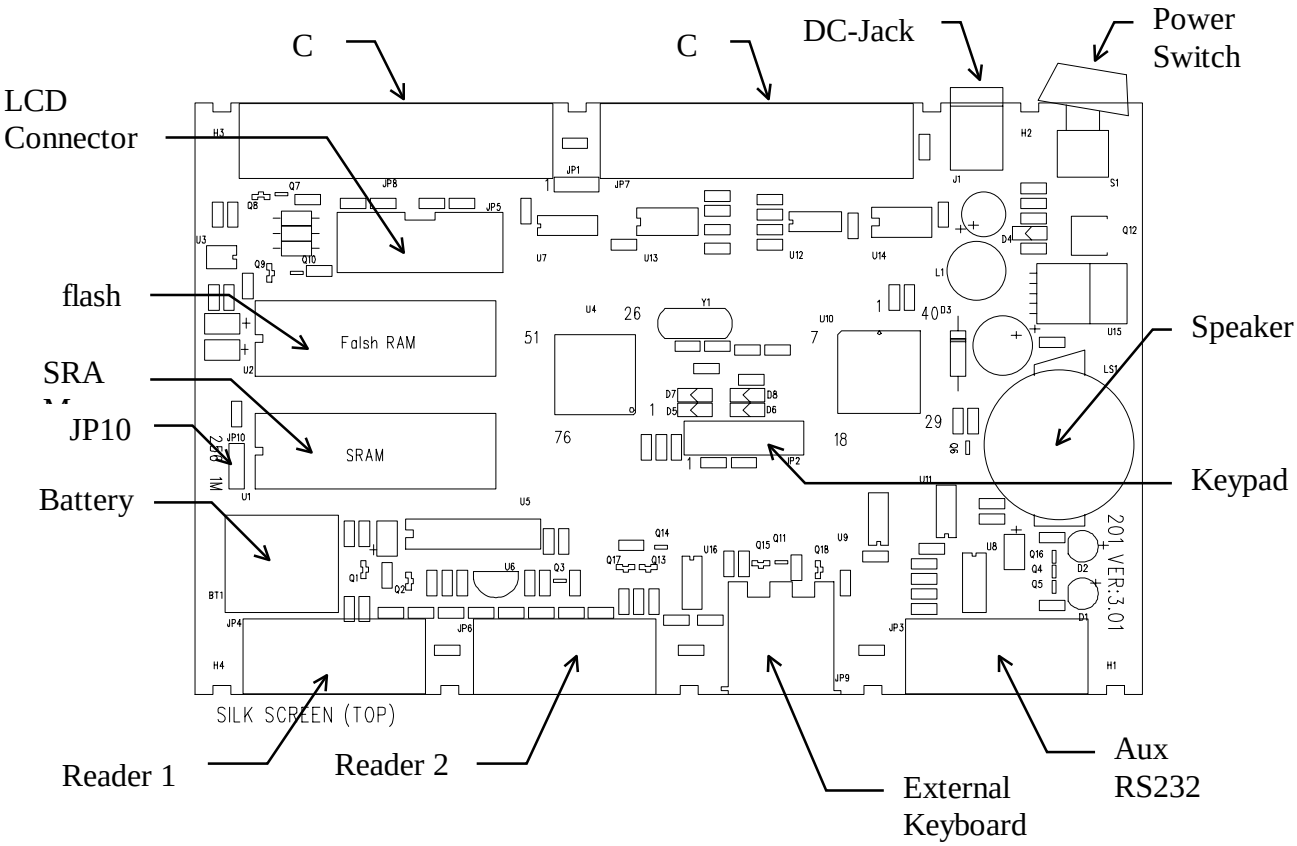


Figure 2. PCB

7. Power Circuit

The 201 can be powered in two ways,

- 8 to 20 V from the DC jack
- +5V from C1 or C2

Later is used mostly for keyboard emulation decoders where the power can be drawn from the host computer. In case this host power is not available or not adequate, an wall adapter (in the range of 8 to 20V) can be fed via the DC-jack. As long as this external power is asserted, the +5V from C1 or C2 is disconnected via an internal FET switch. A simple buck-type switching regulator (LM2575) is followed to generate the required system power, +5V. This regulator is capable of providing up to 1 Amp currents and provides a reasonable typical efficiency around 70% to 80%. Low-ESR (equivalent series resistance) type electrolytic capacitors are used both at input and output sides to reduce ripples.

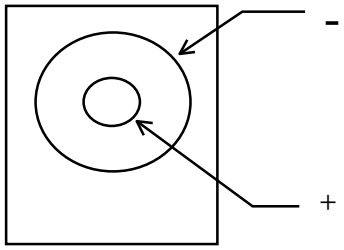


Figure 3. Main Power Connector

The power is controlled via a dual pole dual throw (DPDT) type switch and a resistor is used to discharge the output capacitor when switch was turned off (namely, to the OFF side). As the 201 itself consumes very little power (typical 50mA with LCD back-light off, no external devices attached), this ensures a sharp power up and down sequence.

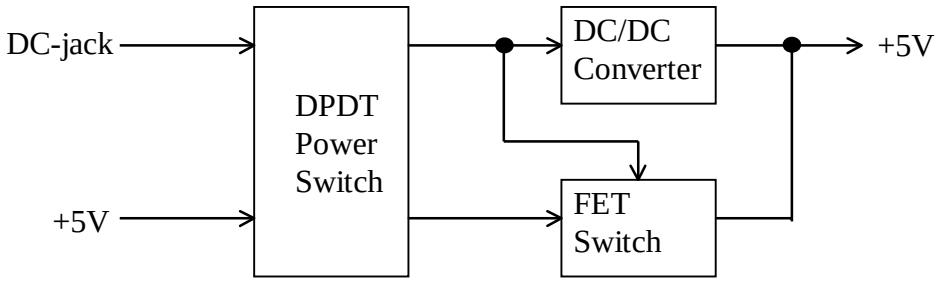


Figure 4. Power Circuit

8. Reset

The system reset signal is generated by a voltage detector chip RICO RE5V or compatible chips. It outputs an active low reset signal when the system power drops below a pre-determined voltage level (Vdet-). The reset signal then changes to high when the power is higher than another pre-determined voltage level (Vdet+). The Vdet+ is about 200 mV higher than Vdet-, this phenomenon known as hysteresis, prevents noise to false-trigger the reset circuitry. The TLCS-900 is guaranteed to work within 5V 10% and the Vdet- is set to 4.6V. This reset signal does not only ensure the proper operation of the CPU but is also used to reset the UART chip (NS82C50) and disables SRAM access (connecting to SRAM CE2) during power-up and power-down. The later is very important as the SRAM contents might be changed by unwanted spikes during supply voltage change.

9. Program Memory (Flash)

128 Kbytes flash memory (U2) is used to store the program code and is guaranteed to last at least 100,000 erase/program cycles. 2 kinds of flash chips can be used, the AMD 29F010 and 28F010 from Intel, MX and so on, and the access time must be 150 ns or faster. The former is a pure +5V device whereas the later requires a +12V for erasing/programming. U3 and accompanying passive components are used to generate this +12V. The U3 can be a Maxim MAX660 or Linear Technology LT1262, which two are total-compatible. Instead of inductor type switching DC/DC converter, these chips utilize a capacitor switching type circuitry and features smaller PCB space, lower ripple and lower EMI emission.

The +12V generation is controlled by a CPU output pin and types of flash memory utilized is automatically identified by software (refer to software manual, routine download()). That is, if 29F010 is used, this circuit is not enabled. During normal read, this DC/DC converter is disabled and the voltage stays at 0V.

10. Data Memory (SRAM)

The data memory can be a 32KB or 128KB SRAM. However, to accommodate different pin assignments, the SRAM type must be selected via the jumper, JP10 as follows,

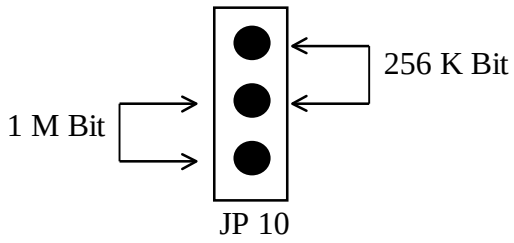


Figure 5. SRAM type selector

Also, the SRAM should be plugged as follows,

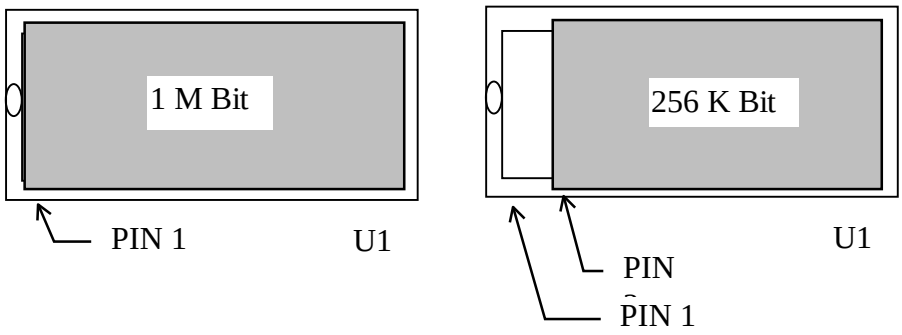


Figure 6. SRAM type connection

The SRAM used must be LL type to reduce battery power consumption and with access time 150 ns or faster. These SRAMs are backup by a NiCd battery and will be described in detail later.

11. Calendar chip

A battery backup calendar chip is used to retain the system time even when power is off. The chip utilized is a V3022 from EM micro-electronic Marin SA. It features the following outstanding features,

- Very low power consumption
  When powered from the battery (3.6V), the current is typically 0.9 μA and maximally 1.5 μA.
- Wide operation voltage range
  This chip works down to 2.0 V.
- On-chip high precision oscillator
  This is a must for accurate time keeping as it is factory trimmed and external oscillators tend to be effected by outside electro-magnetic noise, temperature and so on for the long leads and traces.
- Timer Adjustment
  It can also be fine tuned to compensate for a fast or slow clock. This is an outstanding feature for those applications which need punctual system time such as a time/clock application. The tuning of the calendar chip is done by modifying the value of the **trimming register** of the calendar chip.
- Trimming Register
  The frequency of the calendar chip can be tuned in units of ppm via a digital trimming register. The trimming range is from 0 to 255 ppm. The bigger the value of the trimming register the slower the calendar chip runs. For instance, if the calendar chip is 1 second **slow** in one day then the value of the trimming register should **decrease** 12 to correctly adjust the calendar chip. During system initialization, this register is set to 186.
  1 sec/ 1 day = 1000000 / (24 hours X 60 min X 60 sec) = 11.57 ppm ~= 12 ppm
- Write-protected
  Unless changing calendar time is needed, it is write-protected and won't be accidentally changed.
- Cold start detection
  A cold start bit is set if power loss encountered or first power-on. The software can then recognize this bit and initialize the calendar chip.

12. Memory and Calendar Backup Battery

A 3.6V rechargeable NiCd battery is used to backup the SRAM and keeps the calendar chip running even when system power is off. Its capacity is 60 mAh and is trickle charged with a typical 1.2 mA current. After fully charged, it is able to sustain for more than 15 months. For example,

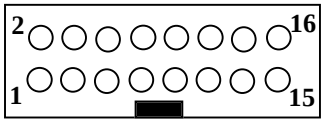
- SRAM (LL-type, SONY CXK581000), current consumed is
  0.7 µA (typical) and 4.0 µA (max., 0 to 40)
- V3022 : 0.9 µA (typical), 1.5 µA (max.)

Time (typical) = 60 mAh / (0.7 + 0.9) = 37500 hrs = 1563 days > 52 months
Time (worst) = 60 mAh / (4.0 + 1.5) = 10909 hrs = 455 days > 15 months

Although behaves in similar ways, unlike system power, switching between +5V and battery is done by 2 transistors and some passive components. This circuit features a very low leakage (base to collector leakage current of the PNP transistor Q1) back to the +5V and a low voltage drop (saturated Vce, ~0.2V). This low drop is necessary for most CMOS chips. If you are interested in this issue, pick up some CMOS chip data sheets. When system power is supplied, the supply voltage for these chips (SRAM & calendar) is +5V - Vdrop. Whereas signals are directly from/to CPU and other chips, which are supplied with +5V. However, for SRAM (a CMOS chip), the upper limit of input signal is Vdd + 0.5V. If using diodes such as 1N4148 for switching, the voltage drop is also 0.6V which is too large and will damage these chips.

13. LCD

An optional 20 X 2 LCD display can be equipped as follows,



20X2, 20X4, 40X2

Figure 7
LCD Connector

1. Ground
2. Vcc, +5V
3. view angle adjust
4. A0
5. A1
6. CS
7. D0
8. D1
9. D2
10. D3
11. D4
12. D5
13. D6
14. D7
15. Back-light Anode
16. Back-light Cathode

Note that although utilizing the same LCD display as the 510, these 2 displays are **not interchangeable**. Signals on the connector are mirrored, this reversal of the power pins will destroy the display.

The LCD is equipped with LED back-light and can be 4 levels tuned. 2 high current NPN transistors (500 mA maximum), Q8 and Q9 are used to drive the back-light and Q8 provides twice current Q9 does. Controlling Q8 & Q9 yields current ratios from 0, 1, 2 to 3.

$$I_{back\text{-}light} = (Vcc - Vce\ (saturated) - Vf) / R$$

Where,

Vcc = supply voltage, +5V
Vce (saturated) = transistor collector to emitter saturation voltage
Vf = LED forward voltage
R = resistor

The typical back-light current is then (5 - 0.2 - 3.8) / 20 = 50 mA. That is, from 0 to 150 mA on a 50 mA basis. As this is an STN-type LCD and the viewing angle is quite large, view angle adjustment is unnecessary.

14. Reader

There are totally 2 reader ports provided, each can be either a Wand, Barcode slot reader, Barcode Scanner with Laser emulation or up to dual-track magnetic card reader. They are equivalent in both hardware and software. Their connectors and pin-assignments are listed below. Beware that in order to decode barcode and magnetic card at the same time, some signals share the same pin. However, the software is able to tell types of the readers attached.

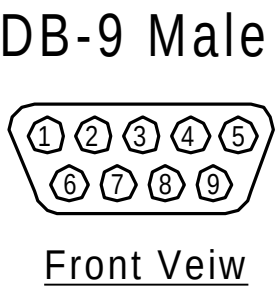
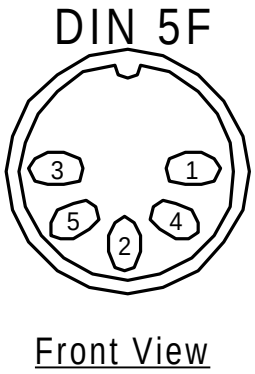


Figure 8. Reader Connector

JP4 & 6	Barcode	Magnetic
1	Start Of Scan	Not used
2	Data	Clock 1
3	Good Read	Not used
4	Not Used	Data 1
5	Switch	Clock 2
6	Power Enable	Not used
7	Ground	Ground
8	Not used	Data 2
9	Vcc, +5V	Vcc, +5V

15. External Keyboard

An external AT-compatible keyboard can be attached for handy data entry. The connector and pin assignment conforms to PC/AT standards.



1. clock
2. data
3. No connection
4. ground
5. +5V

Figure 9. External Keyboard Connector

However, these signals are also used to simulate a keyboard when configured as a wedge-type decoders. In that case, this connector should be left unconnected and the Syntech special wedge cable for that particular wedge emulation should be plugged to C1. Then the original keyboard used by that host computer can be then attached to the special wedge cable.

16. Membrane Keypad

A standard 16-key membrane keypad is provided for data entry.

Figure 10. Keypad Connector

1. In 1
2. In 2
3. In 3
4. In 4
5. Out 1
6. Out 2
7. Out 3
8. Out 4

17. Interface C1

This is a 25 pin D-type female connector as depicted below,

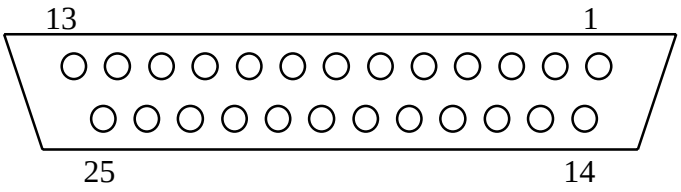


Figure 11. C1

1. Ground
2. TxD 232, transmit data RS232 level
3. RxD 232, receive data RS232 level
4. RTS 232, RTS, RS232 level
5. CTS 232, CTS RS232 level
6. short to C2 pin 6
7. Ground
8. short to C2 pin 8
9. TxD CMOS, transmit data CMOS level
10. RxD COMS, receive data, CMOS level
11. RTS CMOS, RTS, CMOS level
12. CTS CMOS, CTS CMOS level
13. keyboard-emulation signal 1
14. keyboard-emulation signal 2
15. keyboard-emulation signal 3
16. keyboard-emulation signal 4
17. keyboard-emulation signal 5
18. keyboard-emulation signal 6
19. No connection
20. short to C2 pin 20
21. RS485 +
22. RS485 -
23. +5V power input
24. +12V power output, directly from DC-jack
25. +5V power output

It contains the follows,

- Serial communication COM2, one and only one of the follows can be used,
  - RS232
  - CMOS-level RS232
  - RS485
- Wedge emulation
- External power input
- Power pins

17.1. COM2

This communication port can be used as RS485, RS232 or CMOS-level RS232. However as they share the same UART, only one of them can be used at a time. On the software part, the RS232 and CMOS-level RS232 functions the same. For details of the RS-485 usage, please refer to Cipher-510 hardware reference manual.

17.2. Wedge emulation

Up to 6 pins are reserved for keyboard emulation use. When configured as a wedge-emulation decoders, please attach the Syntech specified cable for that particular machine.

17.3. Power Pins

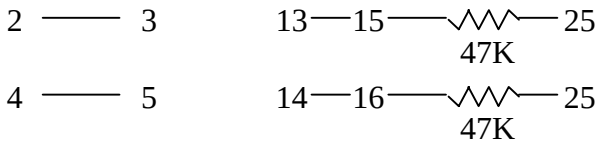
As stated earlier, the 201 can be powered from external +5V through this connector or an unregulated +8V to +20V through the DC-jack.

- Pin 23, +5V power input can be used to draw power from host computer, usually when configured as a decoder. However, as stated earlier, this power source is automatically disconnected by an FET switch if an external power is fed through the DC-jack.
- Pin 24, +12V output : this is the power switch gated power from the DC-jack and can be used to power external devices. However, in doing so, the overall power consumption and adapter power rating must be examined.
- Pin 25, +5V output : this is the power switch gated +5V regulated by the on-board DC-DC converter and can be used to power external devices. However, the on-board regulator is able to supply up to 1 Amp current. In doing so, the overall power consumption must be examined.

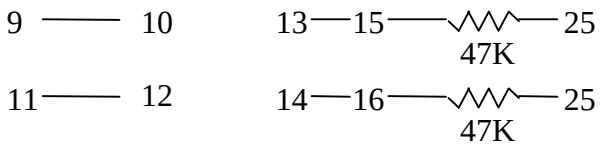
17.4. Loop Back Tester

2 Loop back testers can be used accompanying self-test codes for diagnostics.

- For RS232 & wedge emulation signals,



- For CMOS RS232 & wedge emulation signals,



18. Interface C2

This is a 25 pin D-type male connector as depicted below,

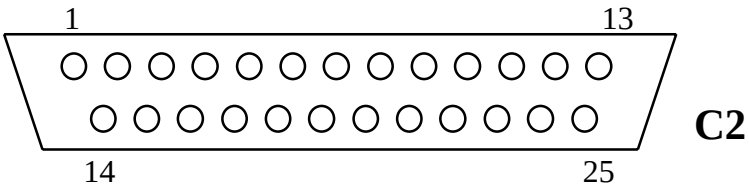


Figure 12. C2

1. Ground
2. RxD 232, receive data RS232 level
3. TxD 232, transmit data RS232 level
4. CTS 232, CTS RS232 level
5. RTS 232, RTS, RS232 level
6. short to C2 pin 6
7. Ground
8. short to C2 pin 8
9. RxD COMS, receive data, CMOS level
10. TxD CMOS, transmit data CMOS level
11. CTS CMOS, CTS CMOS level
12. RTS CMOS, RTS, CMOS level
13. Digital Output 1
14. Digital Output 0
15. Digital Input 1
16. Digital Input 0
17. No connection
18. No connection
19. No connection
20. short to C2 pin 20
21. RS485 +
22. RS485 -
23. +5V power input
24. +12V power output, directly from DC-jack
25. +5V power output

It contains the follows,

- Serial communication COM1, one and only one of the follows can be used,
  - RS232
  - CMOS-level RS232
- Digital Input/output
- External power input
- Power pins

18.1. COM1

This communication port can be used as RS232 or CMOS-level RS232. However as they share the same UART, only one of them can be used at a time. On the software part, the RS232 and CMOS-level RS232 functions the same.

18.2. Digital Input

2 digital inputs are equipped. However, unlike 510, these 2 signals are not photo-isolated and are directly connected to CPU Input pins, thus care must be taken in handling these pins. Also, on the software side, the read value is inverted. That is, if this pin is at high (2.2 ~ 5.3 V), the get_din() will return 0. Whereas 1 is returned if it is at low (-0.3 ~ 1.5V). When floated, 2 on-board pull-up resistors keep these signals at high.

18.3. Digital Output

2 digital outputs are equipped. However, unlike 510, these 2 signals are not photo-isolated and are directly connected to CPU Output pins, thus care must be taken in handling these pins. Also, on the software side, if it is set ON by set_do(), the pin goes to low. Whereas it goes to high when set OFF. The output drive capability is limited as below,

- Output low voltage : maximally 0.45V if sinking 1.6 mA
- Output high voltage : minimally 2.4V if sourcing 400 μA and minimally 3.75V if sourcing 100 μA

Buffering is strongly recommended.

18.4. Power Pins

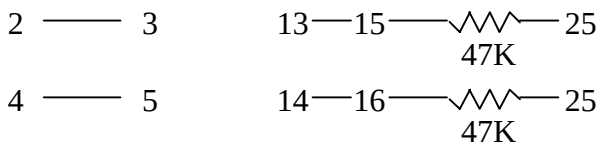
As stated earlier, the 201 can be powered from external +5V through this connector or an unregulated +8V to +20V through the DC-jack.

- Pin 23, +5V power input can be used to draw power from host computer, usually when configured as a decoder. However, as stated earlier, this power source is automatically disconnected by an FET switch if an external power is fed through the DC-jack.
- Pin 24, +12V output : this is the power switch gated power from the DC-jack and can be used to power external devices. However, in doing so, the overall power consumption and adapter power rating must be examined.
- Pin 25, +5V output : this is the power switch gated +5V regulated by the on-board DC-DC converter and can be used to power external devices. However, the on-board regulator is able to supply up to 1 Amp current. In doing so, the overall power consumption must be examined.

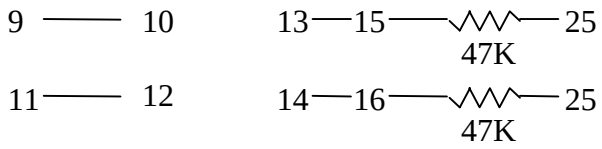
18.5. Loop Back Tester

2 Loop back testers can be used accompanying self-test codes for diagnostics.

- For RS232 & wedge emulation signals,



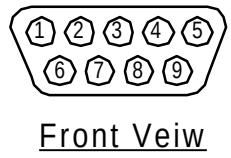
- For CMOS RS232 & wedge emulation signals,



Connection of this tester is identical to that of the C1 except connector polarity. Thus a one to one gender (male to female changer or female to male changer) can be used to swap between C1 and C2.

19. RS232 (COM3)

An auxiliary RS232 is equipped in the front panel as below,



1. No connection
2. Receive data, RS232 level
3. Transmit data, RS232 level
4. No connection
5. Ground
6. No connection
7. RTS, RS232 level
8. CTS, RS232 level
9. +5V

Figure 13. COM3

20. LED

There are totally 2 LEDs on the panel for showing system status.

- READY, Red
- GOOD READ, Green

The GOOD READ LED is activated if one or both of the reader good read LED is activated. That is, these two reader good read signal is Ored to drive this on-board LED.

21. Speaker

A low power speaker is supported and the sound level is 4-level tunable. This speaker electrically behaves like a capacitor, which implies that current flows only when states are changed (charge/discharge capacitor) and very little power is consumed. However, a higher voltage, e.g. 10V is needed to drive it. To do this, the speaker is driven by a pair of complementary CMOS-level 5V signals to produce a virtually 10V peak to peak signals across the speaker. This peak to peak voltage level is altered to control the sound level. Up to 4 sound levels can be set and the corresponding peak to peak voltages are 2.5 V, 5 V, 7.5 V and 10 V. The working frequency ranges from 1KHz to 6KHz and have a peak around 4 KHz.